**Lesson Plan**

**Semester :** 3rd CSE

**Subject :** Digital Electronics Theory & Practical

**Lesson Plan Duration:** 15 weeks

Work Load (Lecture/Practical) per week (in hours): **Lectures 03 hours, Practical 04 hours**

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| **Week** | **Theory** | | **Practical** |
| Lecture Day |  |  |
| 1st | 1 | **MINIMIZATION TECHNIQUES AND LOGIC GATES:** Binary Digits, Logic Levels, and Digital Waveforms, Logic Systems-Positive and negative, Logic Operations ,Active high and Active low concepts | Familiarization with Digital Trainer Kit and associated equipment. |
| 2 | Logical Operators ,Logical Operators, Logic Gates-AND, OR, NOT, NAND, NOR, Exclusive-OR and Exclusive-NOR |
| 3 | Universal Gates and realization of other gates using universal gates |
| 2nd | 4 | Boolean Algebra: Rules and laws of Boolean algebra, Demorgan’s Theorems, Boolean Expressions and Truth Tables, | Study of TTL gates AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR. |
| 5 | Simplification of Boolean Expressions |
| 6 | Standard SOP and POS forms; Minterm and Maxterms, Canaonical representation of Boolean expressions, |
| 3rd | 7 | Minimization Techniques for Boolean Expressions using Karnaugh Map | Design and realize a given function using K-Maps and verify its performance. |
| 8 | Minimization Techniques for Boolean Expressions using Karnaugh Map |
| 9 | Quine McCluskey Tabular method |
| 4th | 10 | Introduction of TTL logic | To verify the operation of Multiplexer and De-multiplexer. |
| 11 | CMOS Logic and their characteristics, Tristate gates. |
| 12 | REVISION |
| 5th | 13 | **COMBINATIONAL CIRCUITS :** Introduction to combinational Circuits, Adders-Half-Adder and Full-Adder, Subtractors- Half and Full Subtractor | To verify the operation of Comparator. |
| 14 | Parallel adder and Subtractor; Look-Ahead Carry Adders. |
| 15 | BCD adder, BCD subtractor, Parity Checker/Generator |
| 6th | 16 | Multiplexer, Demultiplexer, Encoder | To verify the truth table of S-R, J-K, T, D Flip-flops. |
| 17 | Priority Encoder, Comparators. |
| 18 | Decoder ,BCD to Seven segment Display Decoder/Driver LCD Display |
| 7th |  | Minor test |
| 8th | 19 | Introduction to Sequential Circuits, Flip-Flops: Types of Flip Flops -RS, T, D, JK , Edge triggering, Level Triggering; | To verify the truth table of S-R, J-K, T, D Flip-flops. |
| 20 | Flip Flop conversions; Master-Salve JK.; |
| 21 | Introduction to shift registers, Basic Shift Register Operations, types of shift registers , Bidirectional Shift Registers |
| 9th | 22 | Introduction to counters, Types of Counters-Asynchronous and synchronous counters | To verify the operation of Bi-directional shift register. |
| 23 | Up/Down Synchronous Counters, Modulo-n Counter |
| 24 | State table, excitation table concepts |
| 10th | 25 | Design of asynchronous and synchronous counters | To design and verify the operation of 3-bit asynchronous counter. |
| 26 | Ring Counter, Applications of counters. |
| 27 | Revision |
| 11th | 28 | **CONVERTER**  Digital to Analog Converter, Weighed Register: R-2R Ladder Network | To design and verify the operation of asynchronous Up/down counter using J-K FFs.  . |
| 29 | Analog to Digital Conversion, Successive Approximation Type, Dual Slope Type. |
| 30 | Classification of memories - ROM: ROM organization, PROM, EPROM, EEPROM, EAPROM |
| 12th | 31 | RAM: - RAM organization - Write operation, Read operation, Memory cycle, Timing wave forms, memory expansion | To design and verify the operation of asynchronous Up/down counter using J-K FFs. |
| 32 | , Static RAM Cell, MOSFET RAM cell structure, Dynamic RAM cell structure |
| 33 | Programmable Logic Devices - Programmable Logic Array (PLA) Implementation of PLA, |
| 13th | 34 | Programmable Array Logic (PAL), | To design and verify the operation of asynchronous Decade counter. |
| 35 | PAL using ROM. |
| 36 | Revision |
| 14th |  | Minor Test |  |
| 15th | 37 | Revision | To design and verify the operation of asynchronous Decade counter. |
| 38 | Revision |
| 39 | Revision |